REMARKS

The Official Action mailed June 19, 2002 has been received and its contents carefully noted. Claims 12, 13, 16, 18, 19, 23, 24, 27, 29, 30, 32, 34, 41, 53, 55, 58, 65, 66 and 68 are amended herein to further define the presently claimed invention. Claims 12, 13, 15-19, 21-24, 26-43, 46-58, 60, 61, 65-71 and 75-84 remain pending in the present application, of which claims 12, 18, 23, 29, 34, 37, 41, 53, 55, and 58 are independent.

Initially, the undersigned acknowledges with appreciation the courtesies extended by the Examiner during the interview of October 10, 2002.

As discussed during the interview, the present invention is generally directed to a method for fabricating a semiconductor device, comprising the steps of forming an insulating film over the semiconductor film, then crystallizing the entire semiconductor film through the insulating film, including at least a channel formation region of the semiconductor film. The insulating film is then removed and a gate insulating film and gate electrode are formed on the semiconductor film after the insulating film is removed. Boron may also be introduced into at least a portion of the semiconductor film through the insulating film, particularly the portion to become at least a channel region.

The method may also include forming at least two active matrix panels over a substrate wherein each active matrix is formed by the method above. The substrate can then be cut into at least two portions to obtain the at least two active matrix panels. The gate insulating film may further be formed using TEOS. Applicants note that the Examiner takes official notice with respect to this feature, but Applicants request that the Examiner provide evidence of such a feature, particularly with regard to the method of the present invention.

Claims 12, 13, 15, 17, 23, 24, 26, 28-31, 33-39, 41-43, 46, 48-58, 60, 61, 65, 67-71, 75 and 77-84 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Chang, U.S. Patent No. 5,064,775 (Chang), in view of U.S. Patent No. 5,154,946 (Zdebel), further in view of Wolf et al., "Silicon Processing for VLSI Era, Vol. 1: Process Technology" (Wolf) and U.S. Patent No. 4,727,044 (Yamazaki). Further, claims 16, 18, 19, 21, 22, 27, 32, 40, 47, 66 and 76 are

rejected under 35 U.S.C. § 103(a) as being unpatentable over Chang in view of Zdebel and further in view of Wolf and Yamazaki, as applied above, and further in view of U.S. Patent No. 4,599,118 (Han). These rejections are traversed for the reasons advanced in detail below.

The prior art does not teach or suggest all the elements of the claims, either explicitly or inherently. Chang is relied upon for teaching the formation of a semiconductor layer on an insulating surface, introducing B into the semiconductor layer so that the B implanted region becomes at least a part of the channel region, forming a gate insulating film on the semiconductor layer, forming a gate electrode on the a gate insulating film and forming source and drain regions by implanting B into the semiconductor layer using the gate electrode as a mask. Chang fails to disclose forming an amorphous semiconductor film and then converting the same to polysilicon, performing the implant of the channel region through the insulating film, and even more particularly, fails to disclose performing laser crystallization of the semiconductor layer, including at least a channel formation region, through the insulating film.

Yamazaki is relied upon to teach the formation of an insulating film prior to light irradiation. Yamazaki discloses that light 17 is irradiated through a gate insulating layer 3 to active regions 5S' and 5D' to provide source and drain regions 5S and 5D (Figs. 5E to 5G and lines 6 to 66 of column 8). However, Figure 5G and corresponding col. 8, lines 55-68 of Yamazaki disclose that the regions 5S' and 5D' are scanned in their entirety, together with the gate electrode 5G by light 17 (for instance, by an ultra-high mercury lamp), and that the regions 5S' and 5D' are activated, providing source and drain regions 5S and 5D, as well as providing the crystallized regions 6S and 6D.

As a result, it would appear that Yamazaki discloses neither the crystallization using laser nor irradiating the region to become a channel forming region layer, since the light 17 is irradiated through the gate electrode and the gate insulating film 3. That is, only the regions 6S and 6D are irradiated and crystallized, and the channel forming region between the regions 6S and 6D are not irradiated and crystallized because it is masked by the gate electrode. The portion of Yamazaki relied upon by the Examiner at col. 5, lines 49-55 also fails to disclose laser irradiation, but instead only discloses "light" irradiation with the gate electrode already in place, as noted above.

On the other hand, in the presently claimed invention, all independent claims 12, 18, 23, 29, 34, 37, 41, 53, 55 and 58 recite crystallizing the semiconductor film by laser irradiation including, at least, a channel formation region, and then, forming the gate insulating film and gate electrode after the insulating film used for laser irradiation is removed. This means that the entire surface of the semiconductor film is irradiated, rather than only the source and drain regions as provided in Yamazaki.

It should also be noted that laser crystallization provides many advantages, such as allowing the use of many different substrate materials, presenting no problems of strain or shrinkage of substrate, and increasing mobility. (See, page 4, paragraph 2 and page 8, paragraph 2 of the specification). Amorphous silicon TFTs typically provide only a mobility of 0.5 to 1.0 cm^2/Vs (page 24, second paragraph of the specification), while a laser crystallized silicon TFT provides mobility of 60 cm^2/Vs for a N-TFT and 30 cm^2/Vs for a P-TFT (page 20, paragraph 2 and Figures 6A,6B). Further, a TFT having a larger mobility can be obtained at a temperature equivalent to that at which a conventional amorphous silicon TFT is formed (page 12, second paragraph of the specification).

As noted above, the presently claimed invention provides that the insulating film used for laser irradiation is removed and a gate insulating film is then formed. The Office Action contends that Yamazaki is only relied upon to show irradiation through an insulating film, and that previous official notice was taken for replacing the subject insulating film with a new film. Applicants do not accept this contention under official notice, and request that the Examiner provide references to show this feature of the present invention.

None of the cited references disclose this feature of removing the insulating film after laser irradiation, nor the advantages associated with this step in the particular method of the present invention. Specifically, Applicant has recognized that during crystallization from an amorphous state, a considerable amount of non-stoichiometric compounds are often found to develop at an interface between an insulator and a semiconductor. The non-stoichiometric compounds function insufficiently either as insulators or semiconductors. The present invention has the advantage that these non-stoichiometric compounds are removed and a more pure silicon

with favorable crystallinity is obtained since the once provided protective layer is removed. This feature is not taught or suggested by Chang or any of the other cited art of record.

The rejection based on Wolf et al. is also not appropriate as combined with the other cited references. The Examiner is contending that the screen layers of Wolf et al. are not integral parts of the device so they are removed after the process is completed. Wolf et al. appears to disclose, however, that the layer may be present as an integral part of the final device structure, since the reference does not disclose that the layers are removed. As a result, this reference also fails to disclose the removal of the insulating film, since it is not appropriate to assume that the layers are removed with out further disclosure in the Wolf et al. document.

In addition, Chang, as well as the remaining cited references, fail to disclose the formation of at least two active matrix panels over a substrate by first forming the active matrix panels and then cutting the substrate into portions to obtain the two panels. Such a feature permits less fabrication steps, and, thus, improved ability for mass production. As a result, claims 34 and 58 should be further considered to be allowable for reciting these features.

Further, in addition to the features discussed above regarding laser crystallization, claims 18 and 37 recite the feature of providing a tapered channel region as illustrated, at least, in Figures 9A-D and 16A-D. This feature further distinguishes claims 18 and 37, as well as the claims depending therefrom, over the cited art of record.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn and that the application be passed to issue. If the Examiner feels that any further discussions would expedite the prosecution of this matter, he is invited to contact the undersigned.

Respectfully submitted,

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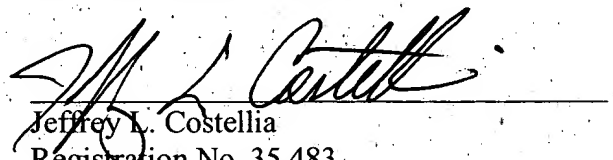

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ATTACHMENT TO THE AMENDMENT

12. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon [on] over an insulating surface;

forming an insulating film on said semiconductor film;

[introducing boron into at least a portion of said semiconductor film though said insulating film, said portion to become at least a channel region;]

crystallizing at least a channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode on said gate insulating film[, said gate electrode having tapered side edges]; and

forming source and drain regions in said semiconductor film by ion doping through said gate insulating film.

13. (Amended) A method according to claim [12] 37 wherein said channel formation region is substantially intrinsic type or p-type.

16. (Amended) A method according to claim [12 wherein said forming said gate electrode is performed by a wet etching.] 58, wherein said channel formation region is substantially intrinsic type or p-type.

18. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon [on] over an insulating surface;

forming an insulating film on said semiconductor film;

[introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;]

crystallizing at least a channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode on said gate insulating film, said gate electrode having tapered side edges; and

forming source and drain regions in said semiconductor film by ion doping[.],

wherein said channel formation region between said source and drain region has a first length at a surface being in contact with said gate insulating film and a second length at a surface being in contact with said insulating surface, and said first length is shorter than said second length.

19. (Amended) A method according to claim [18] 41 wherein said channel formation region is substantially intrinsic type or p-type.

23. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon [on] over an insulating surface;

forming an insulating film on said semiconductor film;

[introducing boron into at least a portion of said semiconductor film though said insulating film, said portion to become at least a channel region;]

crystallizing at least a channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode comprising aluminum on said gate insulating film; and

forming source and drain regions in said semiconductor film by ion doping [which is performed] through said gate insulating film.

24. (Amended) A method according to claim [23] 55 wherein said channel formation region is substantially intrinsic type or p-type.

27. (Amended) A method according to claim [23] 18 wherein said gate electrode is performed by a wet etching.

29. (Amended) A method for fabricating [a thin film transistor of a pixel portion in] a semiconductor device, comprising the steps of:

forming a semiconductor film comprising amorphous silicon [on] over an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel formation region;

crystallizing at least said channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode on said gate insulating film; and

forming source and drain regions in said semiconductor film by ion doping.

30. (Amended) A method according to claim 29 wherein said channel formation region is substantially intrinsic type or p-type.

32. (Amended) A method according to claim [29 wherein said forming said gate electrode is performed by a wet etching] 53 said source and drain regions are formed by said ion doping with at least one of phosphorus and boron.

34. (Amended) A method for fabricating [a thin film transistor of a pixel portion in] a semiconductor device, comprising the steps of:

forming at least two active matrix panels over a substrate, a method for fabricating each of said active matrix panels comprising:

forming a semiconductor film on an insulating surface;

forming an insulating film on said semiconductor film;

[introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel region;].

crystallizing at least a channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode on said gate insulating film; [and]

forming source and drain regions in said semiconductor film by ion doping; and

cutting said substrate into at least two portions to obtain said at least two active matrix panels.

37. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film [on] over an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel formation region;

crystallizing at least said channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode on said gate insulating film, said gate electrode having tapered side edges; and

forming source and drain regions in said semiconductor film by ion doping.

wherein said channel formation region between said source and drain region has a first length at a surface being in contact with said gate insulating film and a second length at a surface being in contact with said insulating surface, and said first length is shorter than said second length.

41. (Amended) A method for fabricating a semiconductor device, comprising the steps of:

forming a semiconductor film [on] over an insulating surface;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion to become at least a channel formation region;

crystallizing at least said channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film by wet etching;

forming a gate insulating film on said semiconductor film after said removing said insulating film;

forming a gate electrode comprising aluminum on said gate insulating film;

forming source and drain regions in said semiconductor film by ion doping through said gate insulating film.

53. (Amended) A method for fabricating a thin film transistor of a pixel portion in a semiconductor device, said semiconductor device having at least one thin film transistor comprising a semiconductor film formed adjacent to a gate electrode with a gate insulating film therebetween, said method comprising the steps of:

forming said semiconductor film over a substrate;

forming an insulating film on said semiconductor film;

[introducing boron into at least a portion of said semiconductor film through said insulating film, said portion becoming at least a channel region of said thin film transistor;]

crystallizing at least a channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film; and

forming source and drain regions in said semiconductor film by ion doping,

[introducing boron into said semiconductor film to form a source region and a drain region,] wherein said gate insulating film is formed using TEOS.

55. (Amended) A method for fabricating a thin film transistor of a pixel portion in a semiconductor device, said semiconductor device having at least one thin film transistor comprising a semiconductor film formed adjacent to a gate electrode with a gate insulating film therebetween, said method comprising the steps of:

forming said semiconductor film over a substrate;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion becoming at least a channel formation region of said thin film transistor;

crystallizing at least said channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film; and

forming source and drain regions in said semiconductor film by ion doping[; and

introducing boron into said semiconductor film to form a source region and a drain region], wherein said gate insulating film is formed using TEOS.

58. (Amended) A method for fabricating [in a thin film transistor of a pixel portion in] a semiconductor device[, said semiconductor device having at least one thin film transistor comprising a crystalline semiconductor film formed adjacent to a gate electrode with a gate insulating film therebetween, said method] comprising the steps of:

forming at least two active matrix panels over a substrate, a method for fabricating each of said active matrix panels comprising:

forming a semiconductor film comprising amorphous silicon over a substrate;

forming an insulating film on said semiconductor film;

introducing boron into at least a portion of said semiconductor film through said insulating film, said portion becoming at least a channel formation region of said thin film transistor;

crystallizing at least said channel formation region of said semiconductor film by laser irradiation through said insulating film;

removing said insulating film;

forming a gate insulating film on said semiconductor film;

forming a gate electrode on said insulating film;

forming source and drain regions in the [crystalline] said semiconductor film by ion doping; and

cutting said substrate into at least two portions to obtain two active matrix panels

[introducing boron into said semiconductor film to form a source region and a drain region,

wherein said gate insulating film is formed using TEOS].

65. (Amended) A method according to claim [12] 58 wherein said gate insulating film comprises TEOS.

68. (Amended) A method according to claim 29 wherein [said gate insulating film comprises TEOS] said semiconductor film is irradiated through said gate insulating film and said gate electrode after forming source and drain regions.